WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

an insulator layer;

a planar transistor formed on a first portion of a semiconductor layer, the first portion of the semiconductor layer overlying the insulator layer, and the first portion of the semiconductor layer having a first thickness; and

a multiple-gate transistor formed on a second portion of the semiconductor layer, the second portion of the semiconductor layer overlying the insulator layer, the second portion of the semiconductor layer having a second thickness, and the second thickness being larger than the first thickness.

2. The semiconductor device of claim 1, wherein the semiconductor layer comprises a material selected from a group consisting of silicon, germanium, silicon germanium, and combinations thereof.

3. The semiconductor device of claim 1, wherein the insulator layer comprises silicon oxide.

4. The semiconductor device of claim 1, wherein the first thickness is less than about 400 angstroms.

5. The semiconductor device of claim 1, wherein the second thickness is greater than about 100 angstroms.

6. The semiconductor device of claim 1, wherein the planar transistor comprises:

a planar channel formed from the first portion of the semiconductor layer;

a gate dielectric overlying at least a portion of the planar channel;

a gate electrode overlying the gate dielectric; and

source and drain regions formed in the first portion of the semiconductor layer oppositely adjacent the gate electrode.

7. The semiconductor device of claim 6, wherein the gate dielectric comprises a material selected from a group consisting of silicon oxide, silicon oxynitride, high-k dielectric material, a dielectric with a relative permittivity larger than about 5, and combinations thereof.

8. The semiconductor device of claim 6, wherein the gate electrode comprises a material selected from a group consisting of a metal, a metallic nitride, a metallic silicide, poly-crystalline silicon, and combinations thereof.

9. The semiconductor device of claim 1, wherein the multiple-gate transistor comprises:

a vertical semiconductor fin formed from the second portion of the semiconductor layer;

a gate dielectric at least partially wrapping around a channel portion of the fin;

a gate electrode overlying the gate dielectric; and

source and drain regions formed in the second portion of the semiconductor layer oppositely adjacent the gate electrode.

10. The semiconductor device of claim 9, wherein the gate dielectric comprises a material selected from a group consisting of silicon oxide, silicon oxynitride, high-k dielectric material, a dielectric with a relative permittivity larger than about 5, and combinations thereof.

11. The semiconductor device of claim 9, wherein the gate electrode comprises a material selected from a group consisting of a metal, a metallic nitride, a metallic silicide, poly-crystalline silicon, and combinations thereof.

12. The semiconductor device of claim 1, wherein corners of the semiconductor layer are rounded at edges of active regions of the planar and multiple-gate transistors.

13. A semiconductor device comprising:

an insulator layer;

a first portion of a semiconductor layer having a first thickness, the first portion of the semiconductor layer overlying the insulator layer;

a second portion of the semiconductor layer having a second thickness, the second portion of the semiconductor layer overlying the insulator layer, and the second thickness being larger than the first thickness;

a first transistor having a first active region formed from the first portion of the semiconductor layer; and

a second transistor having a second active region formed from the second portion of the semiconductor layer.

14. The semiconductor device of claim 13, wherein the first thickness is less than about 400 angstroms, and the second thickness of greater than about 100 angstroms.

15. The semiconductor device of claim 14, wherein the first transistor is a planar transistor, and the second transistor is a multiple-gate transistor.

16. The semiconductor device of claim 13, wherein corners of the first and second active regions are rounded.

17. A semiconductor device comprising:

an insulator layer;

a first portion of the semiconductor layer having a first thickness of less than about 400 angstroms, the first portion of the semiconductor layer overlying the insulator layer;

a second portion of the semiconductor layer having a second thickness of greater than about 100 angstroms, the second portion of the semiconductor layer overlying the insulator layer, and the second thickness being larger than the first thickness;

a first transistor having a first active region formed from the first portion of the semiconductor layer; and

a second transistor having a second active region formed from the second portion of the semiconductor layer.

18. The semiconductor device of claim 17, wherein the first transistor is a planar transistor, and the second transistor is a multiple-gate transistor.

19. A method of fabricating a semiconductor device comprising:

forming a first thickness of a first portion of a semiconductor layer, and a second thickness of a second portion of the semiconductor layer larger than the first thickness, wherein the semiconductor layer is overlying an insulator layer;

forming a first active region for a first transistor from the first portion of the semiconductor layer; and

forming a second active region for a second transistor from the second portion of the semiconductor layer.

20. The method of claim 19, wherein the forming of the first and second active regions comprises:

providing a patterned active region mask over the semiconductor layer; and

removing material from the semiconductor layer in alignment with the active region mask to form the first active region in the first portion and to form the second active region in the second portion.

21. The method of claim 19, wherein the first transistor is a planar transistor and wherein the second transistor is a multiple-gate transistor.

22. The method of claim 19, further comprising:

forming a first gate dielectric over a first channel region of the first active region;

forming a first gate electrode over the first gate dielectric;

doping portions of the first active region to form source and drain regions for the first transistor;

forming a second gate dielectric over a second channel region of the second active

region;

forming a second gate electrode over the second gate dielectric; and

doping portions of the second active region to form source and drain regions for the second transistor.

23. The method of claim 22, wherein at least part of the doping of the first and second active regions is performed after the forming of the first and second gate electrodes.

24. The method of claim 22, wherein at least part of the doping of the first and second active regions is performed before the forming of the first and second gate electrodes.

25. The method of claim 22, wherein the first and second gate dielectrics are formed from a same material.

26. The method of claim 22, wherein the first and second gate electrodes are formed from a same material.

27. The method of claim 19, wherein the semiconductor layer comprises silicon, and wherein the forming of the first thickness of the first portion of the semiconductor layer comprises:

providing a patterned mask that covers at least part of the second portion and is open over at least part of the first portion;

oxidizing an exposed top portion of the first portion to form silicon oxide;

removing the silicon oxide; and

removing the mask.

28. The method of claim 19, wherein the forming of the first and second active regions is performed after the removing of the part of the first portion to provide the first thickness of the first portion.

29. The method of claim 19, wherein the forming of the first and second active regions is performed before the removing of the part of the first portion to provide the first thickness of the first portion.

30. The method of claim 19, wherein the second active region is a fin with a fin height of more than about 100 angstroms and a fin width of less than about 500 angstroms.

31. The method of claim 19, wherein the second active region is a fin with a fin height of more than about 400 angstroms and a fin width of less than about 500 angstroms.

32. The method of claim 19, wherein the forming of the first and second active regions comprises:

forming an active region mask to expose selected regions of the first and second portions; and

forming trenches in the selected regions to define the first and second active regions.

33. The method of claim 32, further comprising:

filling the trenches with a dielectric material; and

removing the active region mask.

34. The method of claim 19, wherein the semiconductor layer comprises a material selected from a group consisting of silicon, germanium, silicon germanium, and combinations thereof.

35. The method of claim 19, further comprising:

forming rounded corners on the first and second active regions.

36. The method of claim 35, wherein at least some of the rounded corners have a radius of curvature between about 10 angstroms and about 200 angstroms.

37. The method of claim 35, wherein the forming of the rounded corners is performed using an anneal in a hydrogen-containing ambient with a pressure between about 5 and about 20 Torr, for a duration of between about 15 and about 35 seconds, at a temperature between about 800 and about 1000 degrees Celsius.